National Semiconductor

26075

TP53130 DTMF (TOUCH-TONE) Generator with Binary Data and Keypad Interface

General Description

The TP53130 is a low threshold voltage, ion-implanted, metal-gate CMOS integrated circuit that generates all dual tone multi-frequency (DTMF) pairs required in tone-dialing systems. The 8 audio output frequencies are generated from an on-chip 3.579545 MHz master oscillator. No external components other than the crystal are required for the oscillator. The TP53130 can be powered directly from telephone lines over wide range loop conditions. The device can interface directly to an inexpensive single-contact calculator type keyboard or a standard telephone 2-of-8 keypad *(Figure 4)*. The TP53130 is also capable of accepting binary code inputs for microprocessor-controlled systems applications.

Features

- 3V–15V operating voltage
- On-chip 3.579545 MHz crystal-controlled oscillator
- Tone accuracy better than ± 1% without tuning
- Interface with standard 2-of-8 telephone keypad
- Interface with single-contact low cost keypad
- Input signals can be in binary code
- Multi-key lockout with/without single tone capability
- On-chip high band and low band tone generators and mixer
- High band pre-emphasis
- Low harmonic distortion
- Open emitter-follower low impedance output
- Separate receiver mute and transmitter mute switch outputs
- Powered directly from the telephone line

Block Diagram

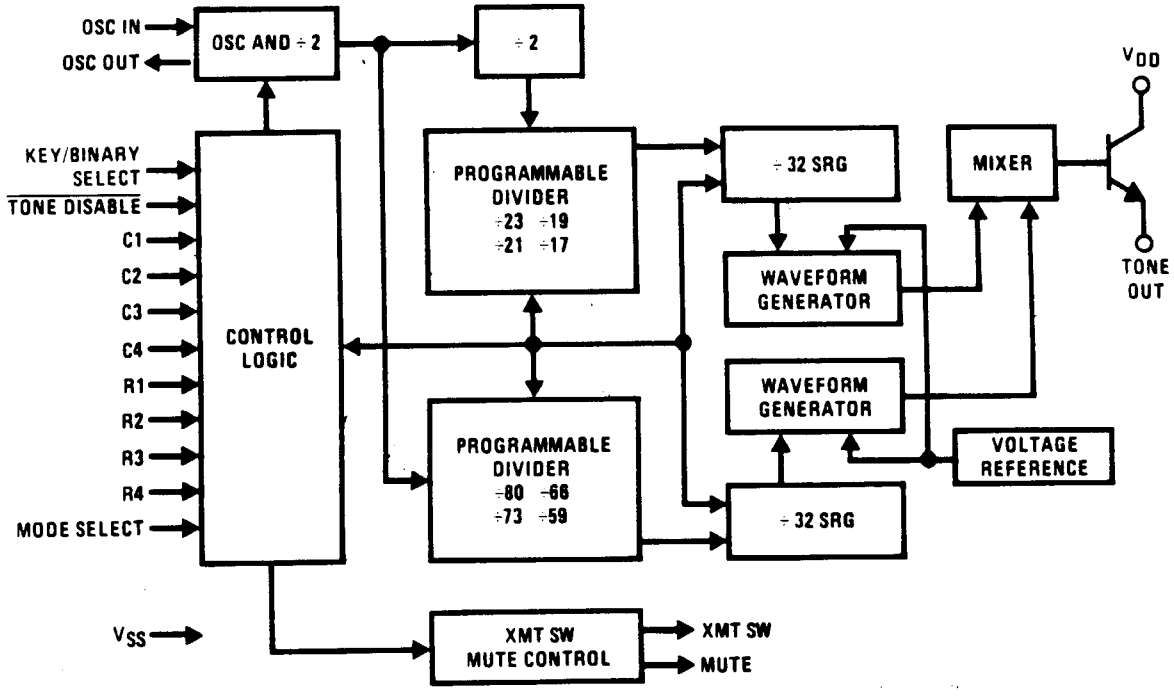


FIGURE 1

Absolute Maximum Ratings

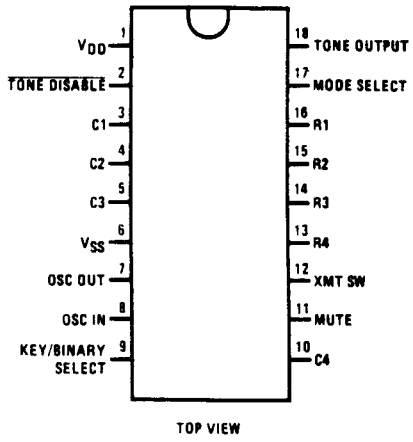
Voltage at Any Pin Except XMT SW and MUTE	V_{SS} − 0.3V to V_{DD} + 0.3V	Operating Temperature Range	− 40°C to + 70°C
Voltage at XMT SW and MUTE Pins	V_{SS} − 0.3V to 15V	Storage Temperature Range	− 65°C to + 150°C
		V_{DD}-V_{SS}	15V
		Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics T_A within operating temperature range, $3V \le V_{DD} \le 8V$, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Input Pull-Up Resistor					
Column and Row Inputs		25	50	90	kΩ
Key/Binary Select		200	650	1000	kΩ
Mode Select		200	650	1000	kΩ
Tone Disable		200	650	1000	kΩ
Input Pull-Down Resistor					
Column and Row Inputs	V_{DD} = 3V	650			Ω
	V_{DD} = 8V	200			Ω
Input Voltage Levels					
Logical "1"		80% of V_{DD}		V_{DD}	V
Logical "0"		V_{SS}		20% of V_{DD}	V
Operating Frequency			3.579545		MHz
Output Voltage Swing at Tone Output					
Low Band Alone	$R_L > 150\Omega$		820		mVp-p
High Band Alone	$R_L > 150\Omega$		1000		mVp-p
Harmonic Distortion	$R_L > 150\Omega$			− 20	dB
Tone Frequency Deviation				1.0	%
Typical Application Output	$20 < I_L < 100$ mA				
Level V_L (See *Figure 5*)					
Low Band Tone	$R_L = 150\Omega$		− 6		dBV
High Band Tone	$R_L = 150\Omega$		− 4		dBV
THD	f ≤ 20 kHz		4		%
Output Currents	V_{DD} = 3V				
XMT SW/MUTE	V_{OUT} = 2V	3			mA
Idle Current	$R_L = \infty$, V_{DD} = 8.0V (No Key Depressed)			1	mA
Operating Current	$R_L = \infty$, V_{DD} = 3.5V			2	mA
Key Down to Tone Outputting Time (Debounce)			3	4	ms
DC Output	Tone Disable = 0		TRI-STATE®		

Connection Diagram

Dual-In-Line Package



Order Number TP53130N
See NS Package N18A

FIGURE 2

Functional Description

A functional block diagram of the TP53130 is shown in *Figure 1*, and connection diagram is shown in *Figure 2*. The TP53130 can be operated in the Keyboard Interface Mode and can also be operated in the Binary Interface Mode depending on the logic level at the KEY/BINARY SELECT input. In either mode, the device will digitally synthesize the high and low band sine waves of DTMF signaling, when valid signals are applied to row and/or column inputs. The sum of the two sine waves is then provided at the Tone output.

TONE DISABLE: This input has an internal pull-up resistor. When this input is open or at logical high (V_{DD}), the XMT SW and MUTE outputs will deliver valid output signals in response to the proper input signals. When TONE DISABLE is at logical low (V_{SS}), the device will be in the inactive mode. Tone output will go to an open circuit state, XMT SW and MUTE outputs will sink current through on-chip N-channel devices and the crystal oscillator will be disabled.

KEY/BINARY SELECT: When this input is open or at logical high (V_{DD}), the device will interface a keyboard. (See Table I.) When KEY/BINARY SELECT is low (V_{SS}), the device will accept binary inputs on the row signal input lines. (See Table II.)

OSC IN, OSC OUT: Tone generation and internal timing are dependent on the accurate operation of the crystal oscillator. The oscillator inverter/amplifier and all necessary bias networks are included on-chip. The only external component is a 3.579545 MHz crystal. It should be connected to the device as shown in the typical application diagram *(Figure 5)*. The oscillator is not running unless a valid input signal is applied to the device. The oscillator is also disabled when TONE DISABLE is tied to logic low (V_{SS}). This feature will prevent RF modulation on the telephone line.

Single Tone Capability: This is a desirable feature for initial testing. With the device operating in the Keypad Interface Mode, operation of multiple keys in different rows and columns will not generate output tones. However, operation of two or more keys in the same row or column will generate the proper tone for that row or column. During multiple key operation, the XMT SW and MUTE outputs will not change state more than once. With the device operating in the Binary Interface Mode, a logical low at the column 1 input will inhibit the high band tone output while a logical low at the column 2 input will inhibit the low band tone output. (See Table I.) Logical low inputs on both column inputs 1 and 2 will disable the device the same way as the TONE DISABLE input will when set to logical low.

MODE SELECT: This input has an internal pull-up resistor. When open or at logical high, single tone outputs are allowed. When this input is at logical low, single tone outputs are prohibited. XMT SW and MUTE outputs will stay high during a multiple key depression input.

TONE OUTPUT: Dual-tone output frequencies are generated in response to valid input signals to the device. See Table III.) Each frequency is synthesized with 32 steps of approximation for low harmonic distortion. The amplitudes of the low and high frequency tones are constant and independent of operating voltages. When tone outputs are present, the Tone output will be the composite of the AC signal superimposed on a DC offset. The DC offset is approximately 1/2 V_{DD}. When no tones are present at the Tone output pin, the pin will be open circuit.

XMT SW (Transmitter Switch) and MUTE Outputs: In the idle state (no key depressed, no signal interface inputs and TONE DISABLE at a logical low) both the XMT SW and MUTE outputs will sink current to V_{SS} through on-chip transistors. In the active state, these outputs will source current from V_{DD} whenever valid output tones are generated. The MUTE output activates before the XMT SW output as shown in *Figure 3*.

Signal Inputs (Row and Column Inputs): An input scan technique is used so that the device can directly interface either 2-of-8 keypads with common switch arrangements or the single contact X-Y keypads when KEY/BINARY SELECT is open circuit. (See *Figure 4*.)

Functional Description (Continued)

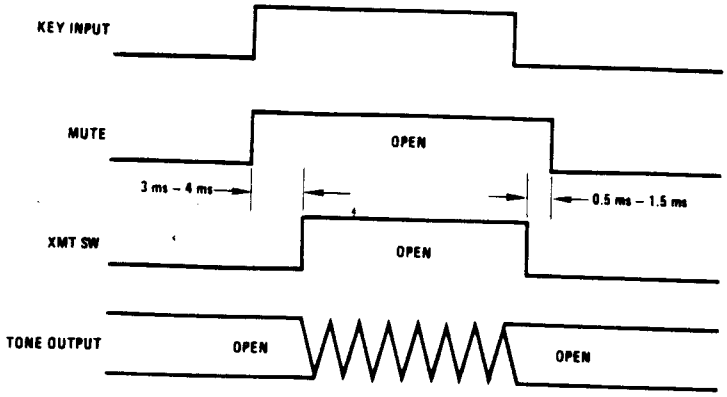


FIGURE 3. Timing Diagram of MUTE and XMT SW in Relation to Key Input and Tone Output

TABLE I. Functional Truth Table (With "MODE SELECT" Open)

Key/Binary Select	Tone Disable	Row	Column	Tone Output		XMT SW	MUTE
				Low Band	High Band		
X	0	X	X	0	0	0	0
1	1	One	One	f_L	f_H	1	1
1	1	One	Two or More	f_L	0	1	1
1	1	Two or More	One	0	f_H	1	1
1	1	Two or More	Two or More	0	0	0	0
0	1	Binary	Open	f_L	f_H	1	1
0	1	Binary	C1 = 0	f_L	0	1	1
0	1	Binary	C2 = 0	0	f_H	1	1
0	1	X	C1 and C2 = 0	0	0	0	0

TABLE II. Functional Truth Table for Binary Interface

Keyboard Inputs	Binary Inputs						Frequencies Generated	
	C1	C2	R1	R2	R3	R4	f_L (Hz)	f_H (Hz)
1	Open	Open	0	0	0	1	697	1209
2	Open	Open	0	0	1	0	697	1336
3	Open	Open	0	0	1	1	697	1477
4	Open	Open	0	1	0	0	770	1209
5	Open	Open	0	1	0	1	770	1336
6	Open	Open	0	1	1	0	770	1477
7	Open	Open	0	1	1	1	852	1209
8	Open	Open	1	0	0	0	852	1336
9	Open	Open	1	0	0	1	852	1477
0	Open	Open	1	0	1	0	941	1336
*	Open	Open	1	0	1	1	941	1209
#	Open	Open	1	1	0	0	941	1477
A	Open	Open	1	1	0	1	697	1633
B	Open	Open	1	1	1	0	770	1633
C	Open	Open	1	1	1	1	852	1633
D	Open	Open	0	0	0	0	941	1633
	0	Open	Valid Binary Inputs				f_L	—
	Open	0					—	f_H
	0	0					1/2 V_{DD}	1/2 V_{DD}

Functional Description (Continued)

TABLE III. Output Frequencies

Inputs	Desired Freq. (Hz)		Actual Frequency (Hz)	Percent Deviation
	f_L	f_H		
R1	697		699.1	0.306
R2	770		766.2	−0.497
R3	852		847.4	−0.536
R4	941		948.0	0.741
C1		1209	1215.9	0.569
C2		1336	1331.7	−0.324
C3		1477	1471.9	−0.35
C4		1633	1645.0	0.736

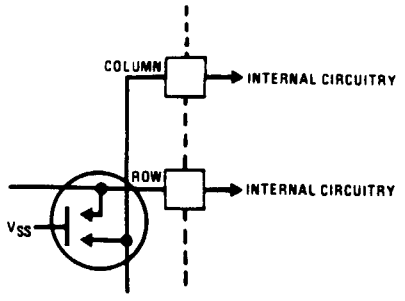


FIGURE 4a. Standard Dual Contact Telephone Key

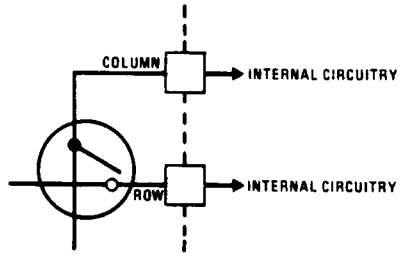
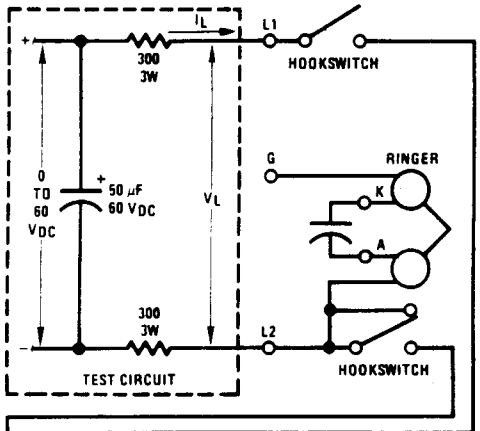


FIGURE 4b. Single Contact Key

Typical Application



Note 1: All resistances are in ohms.

Note 2: Test circuit used to measure signal levels and distortion.

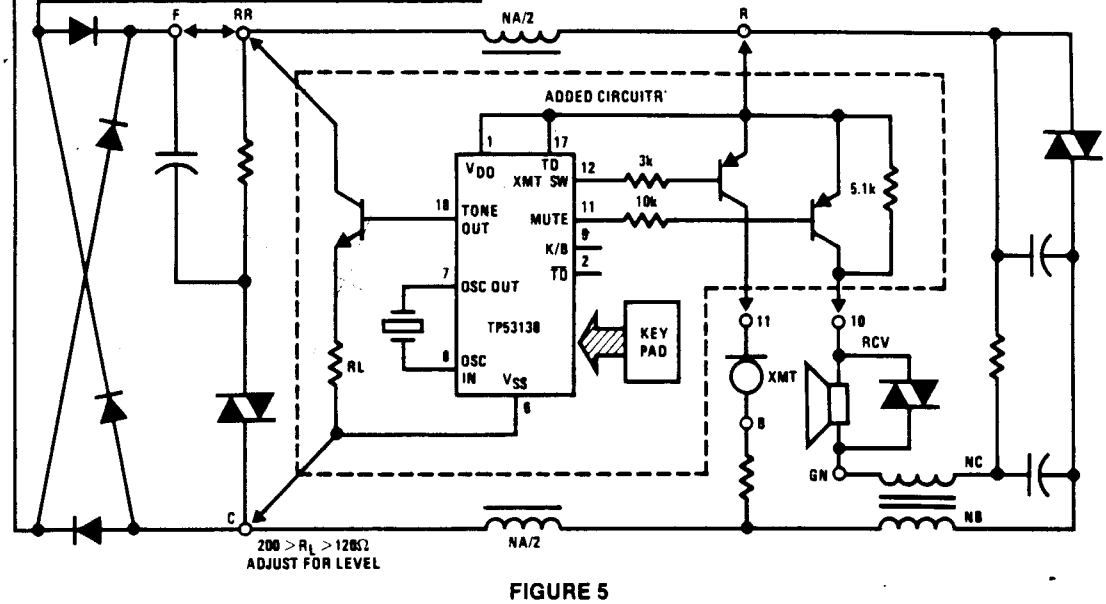


FIGURE 5